

**In the claims:**

For the Examiner's convenience, all pending claims are presented below with changes shown.

- 1 1-3 (Cancelled)
- 1 4. (Currently Amended) A computer system comprising:
- 2 a central processing unit (CPU) having:
- 3 a CPU core;
- 4 cache memory having a plurality of cache lines, each of the plurality of
- 5 cache lines being compressible to form compressed cache lines to store additional
- 6 data; and
- 7 compression/decompression logic; and
- 8 a memory controller coupled to the CPU having a compression map to indicate
- 9 whether a cache line corresponding to a block of data in a system memory is in a
- 10 compressed format, and a type of compression used for each cache line stored in a
- 11 compressed format.
- 1 5. (Previously Presented) The computer system of claim 4 wherein the
- 2 compression map includes bits that provides status for each aligned block in the system
- 3 memory.
- 1 6. (Previously Presented) The computer system of claim 4 wherein the
- 2 compression/decompression logic compresses cache line data with a companion cache
- 3 line as the data is passed from the CPU core to the cache memory.

1 7. (Previously Presented) The computer system of claim 4 wherein the  
2 compression/decompression logic compresses cache line data with a companion cache  
3 line prior to the data being passed to the system memory.

1 8. (Previously Presented) The computer system of claim 4 wherein the  
2 compression/decompression logic compresses cache line data with a companion cache  
3 line prior to the data being passed to a second CPU.

1 9. (Previously Presented) The computer system of claim 4 wherein CPU  
2 further comprises a buffer to temporarily store cache line data prior to the data being  
3 compressed at the compression/decompression logic.

1 10. (Previously Presented) The computer system of claim 4 further comprising:  
2 a first interface to communicate with components that transmit and receive  
3 uncompressed cache line data; and  
4 a second interface to communicate with components that transmit and receive  
5 compressed cache line data.

1 11. (Previously Presented) The computer system of claim 4 further comprising  
2 cache coherency logic.

1 12. (Currently Amended) A method comprising:  
2 compressing one or more of a plurality of cache lines to form one or more  
3 compressed cache lines; and

4 updating a compression map a within a memory controller to indicate the one or  
5 more cache lines corresponding to a block of data in a system memory are in a  
6 compressed format, and to indicate a type of compression used for each cache line stored  
7 in a compressed format.

1 13. (Previously Presented) The method of claim 12 further comprising storing  
2 the compressed cache lines in a cache memory.

1 14. (Previously Presented) The method of claim 12 wherein updating the  
2 compression map comprises updating a status bit associated with the block of data.

1 15. (Previously Presented) The method of claim 12 further comprising  
2 buffering data corresponding to the cache lines prior to compressing the cache lines.

1 16. (Previously Presented) The method of claim 13 further comprising  
2 transmitting the compressed cache lines to the system memory.

1 17. (Currently Amended) A central processing unit (CPU) comprising:  
2 a CPU core;  
3 a cache memory having a plurality of cache lines, each of the plurality of cache  
4 lines being compressible to form compressed cache lines to store additional data;  
5 compression/decompression logic; and  
6 a memory controller having a compression map to indicate whether a cache line  
7 corresponding to a block of data in a system memory is in a compressed format, and a  
8 type of compression used for each cache line stored in a compressed format.

1 18. (Previously Presented) The CPU of claim 17 wherein the compression map  
2 includes bits that provides status for each aligned block in the system memory.

1 19. (Previously Presented) The CPU of claim 17 wherein the  
2 compression/decompression logic compresses cache line data with a companion cache  
3 line as the data is passed from the CPU core to the cache memory.

1 20. (Previously Presented) The CPU of claim 17 wherein the  
2 compression/decompression logic compresses cache line data with a companion cache  
3 line prior to the data being passed to the system memory.

1 21. (Previously Presented) The CPU of claim 17 wherein the  
2 compression/decompression logic compresses cache line data with a companion cache  
3 line prior to the data being passed to a second CPU.

1 22. (Previously Presented) The CPU of claim 17 wherein CPU further  
2 comprises a buffer to temporarily store cache line data prior to the data being compressed  
3 at the compression/decompression logic.

1 23. (Previously Presented) The CPU of claim 17 further comprising:  
2 a first interface to communicate with components that transmit and receive  
3 uncompressed cache line data; and  
4 a second interface to communicate with components that transmit and receive  
5 compressed cache line data.